



Intel® E7500 Chipset Memory Controller Hub (MCH)

Specification Update

December 2002

Notice: The Intel® E7500 MCH may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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Contents

Revision History	4
Preface.....	5
Specification Changes	9
Errata	11
Specification Clarifications	13
Documentation Changes	15

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	February 2002
-002	Added A3 Spec Number	December 2002

Preface

This document is an update to the specifications contained in the *Intel® E7500 Chipset Datasheet: E7500 Memory Controller Hub (MCH)* (document number 290730). It is a compilation of device/document errata and specification clarifications/changes, and is intended for hardware system manufacturers and software developers of applications, operating system, and tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® E7500 MCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® E7500 MCH may be identified by the following register contents:

Stepping	Vendor ID ¹	Device ID ²	Revision Number ³
A2	8086h	2540h	02h
A3	8086h	2540h	03h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® E7500 MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A2	SL64H	RGE7500PL	Production
A3	SL69U	RGE7500PL	Production

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® E7500 MCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Erratum, Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

Fix: This erratum is intended to be fixed in a future stepping of the component.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Eval: Plans to fix this erratum are under evaluation.

Other

Shaded: This item is either new or modified from the previous version of the document.

NO.	SPECIFICATION CHANGES
1	There are no specification changes in this Specification Update Revision

NO.	A2	A3	PLANS	ERRATA
1	X		Fixed	System Bus Strobe Glitch Falsely Reported (Partial Fix)
2	X		Fixed	Data Corruption In Mixed x4 / x8 DIMM Configurations

NO.	SPECIFICATION CLARIFICATIONS
1	Section 3.6.16 DRAM Row Boundary Register
2	Section 4.1 System Memory Spaces

NO.	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision



Specification Changes

There are no documentation changes in this Specification Update revision.

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Errata

1. System Bus Strobe Glitch Falsely Reported

Problem: The Intel® E7500 Chipset MCH logic that monitors the system bus for data strobe glitches incorrectly detects a glitch even though no glitch has occurred.

Implication: SYSBUS_FERR bit [1], SYSBUS_NERR bit [1], and FERR_GLOBAL bit [16] will falsely report that a system bus error has been detected. Clearing these bits is not possible, as they are incorrectly set on every system bus transaction.

Workaround: Monitor SYSBUS_NERR for system bus errors, ignoring bit [1].

Status: Fixed in the MCH A3 stepping.

2. Data Corruption In Mixed x4 / x8 DIMM Configurations

Problem: Read data on the DDR memory interface is latched into an input FIFO using either all of the DQS signals (when reading from a DIMM with x4 devices) or only the lower half of the DQS signals (when reading from a DIMM with x8 devices). When a system is populated with both x4 and x8 DIMMs, an internal MUX is used to switch between using all or half of the DQS signals to latch the FIFO (depending on which DIMM is being accessed). When the internal MUX select signal switches, the MUX outputs may incorrectly signal the FIFO to latch data.

Implication: Data corruption has been observed on the DDR memory interface when system configurations include mixing of x4 and x8 DIMM types.

Workaround: Populate homogenous DIMM configurations only (all x4 DIMMs or all x8 DIMMs)

Status: Fixed in the MCH A3 stepping.



Intel® E7500 Memory Controller Hub (MCH)

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Specification Clarifications

1. **Section 3.6.16 DRAM Row Boundary Register**

Locked cycles to out of bounds memory locations (i.e. – locations above the top of total memory) are not supported. Typically both locked and unlocked cycles to out of bounds memory locations will result in all 1s being returned on the system bus. Infrequently, however, locked cycles to these regions can result in unpredictable Intel® E7500 Chipset MCH behavior.

2. **Section 4.1 System Memory Spaces**

Locked cycles to out of bounds memory locations (i.e. – locations above the top of total memory) are not supported. Typically both locked and unlocked cycles to out of bounds memory locations will result in all 1s being returned on the system bus. Infrequently, however, locked cycles to these regions can result in unpredictable Intel® E7500 Chipset MCH behavior.



Intel® E7500 Memory Controller Hub (MCH)

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Documentation Changes

There are no documentation changes in this Specification Update revision.